Amendments to the Claims

This listing of the claims will replace all prior versions, and listings, of claims in the application.

1-4. (Withdrawn)

5. (Previously Presented) A timing generation module for use in a data communications system, said timing generation module comprising:

a first variable modulus counter having a first clock input, a first control input, and a first variable modulus counter output, said first clock input to be coupled to a transmitter clock, said first variable modulus counter operable to divide the transmitter clock frequency by a first adjustable integer;

a second variable modulus counter having a second clock input, a second control input, and a second variable modulus counter output, said second clock input to be coupled to a network link clock, the network link clock frequency having a predetermined relationship with the transmitter clock frequency, said second variable modulus counter operable to divide the network link clock frequency by a second adjustable integer;

wherein said first adjustable integer is selected to a first value and the second adjustable integers is selected to be a second value such that the quotient of the transmitter clock frequency divided by the first value is substantially the same as the quotient of the network link clock frequency divided by the second value,

a phase detector module comprising one or more D flip-flops, the phase detector module couple-able to the first clock input and the second clock input to generate one or more data bits to indicate a phase offset between the first clock input and the second clock input; and

a modulus control module responsive to one or more data bits to indicate a phase offset to control said first and second variable modulus counters.

6-8. (Withdrawn)

9. (Currently Amended) A timing generation module as recited in claim 5, wherein said timing generation module ~~network link clock~~ is further operable to transmit said one or more data bits to indicate the phase offset ~~said quantized bit~~ in an overhead channel.

10-11. (Withdrawn)

12. (Currently Amended) A timing generation module as recited in claim 5, wherein said ~~transmitter circuit~~ timing generation module is one component of a high speed modem.

13. (Currently Amended) A receiver circuit for use in a data communications system, said receiver circuit operable to receive timing data and to recover transmit timing data ~~and synchronize received data according to recovered transmit timing data~~, said receiver circuit comprising:

a first variable modulus counter controllable to frequency divide a first input signal by a first integer adjustable by an arbitrary integer offset +/-N to generate a first output signal;

a second variable modulus counter controllable to frequency divide a second input signal by a second integer adjustable by an arbitrary integer offset +/-M to generate a second output signal;

a detector circuit operable to determine a phase relation between said first and second output signals;

an oscillator circuit controlled by said phase relation, said oscillator providing feedback to said second variable modulus controller;

a modulus control circuit responsive to received timing data, said modulus control circuit operable to control said first and second variable modulus counters,

whereby said receiver circuit~~ry~~ reaches a steady state and recovers the transmit timing data. ~~generates a clock signal for synchronizing received data based on recovered phase variation information~~.

14. (Currently Amended) A receiver circuit as recited in claim 13 further comprising:

a circuit for receiving ~~primary transmitted~~ timing data; and another circuit~~ry~~ for recovering received timing data.

15. (Previously Presented) A receiver circuit as recited in claim 13 further comprising:

a lowpass filter coupled between said detector circuit and said oscillator circuit.

16-18. (Withdrawn)

19. (Currently Amended) A method, of signal generation, the method, comprising: ~~as recited in claim 16,~~

providing a master clock signal and a network link clock signal determining a phase relation between said master clock signal and said network link clock signal; and

re-generating the master clock signal based on the phase relation and the network link clock signal;

wherein said master clock signal and said network link clock signal have a predetermined relation defined by a first adjustable integer and a second adjustable integer, wherein the determining said phase relation includes:

determining a first value for the first adjustable integer and determining a second value for the second adjustable integer such that the quotient of a master clock signal frequency divided by the first value is substantially the same as the quotient of a network link clock signal frequency divided by the second value;

dividing said master clock signal frequency by the first value to generate a first signal of a first frequency;

dividing said network link clock signal frequency by the second value to generate a second signal of a second frequency; wherein the first frequency and the second frequency are substantially equal to a reference frequency value;

comparing said first signal with said second signal to determine the phase relation; and

adjusting one or more of a value of the first adjustable integer and a value of the second adjustable integer based on the phase relation.

20. (Currently Amended) A method, of signal generation, the method, comprising: ~~as recited in claim 19,~~

providing a master clock signal and a network link clock signal determining a phase relation between said master clock signal and said network link clock signal; and

re-generating the master clock signal based on the phase relation and the network link clock signal; wherein said phase relation is quantized.

21. (Currently Amended) [[A]] The method, of claim 20: ~~as recited in claim 19,~~

wherein said phase relation is transmitted via an overhead channel at a frequency no larger than the reference frequency value.

22. (Previously Presented) The timing generation module of claim 5, further comprising a phase accumulator module coupled to an output of the phase detector module.

23. (Previously Presented) The timing generation module of claim 22, further comprising a register having an output port to be coupled to an input port of the phase accumulator module, the register to be adjustable to determine a phase offset correction resolution.

24. (Previously Presented) The timing generation module of claim 22, wherein the phase accumulator module is coupled to a delta-sigma modulator.